# Advanced CMOS TTL Input – 54ACT08

**Quad 2-Input AND Gate in bare die form**

**Rev 1.0**
**17/09/25**

## Description

The 54ACT08 quad 2-input AND gate is fabricated using an advanced 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device consists of four independent 2-input AND gates with standard push-pull outputs and performs the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$. Device inputs are compatible with standard CMOS outputs and also directly compatible with LSTTL outputs. All inputs are protected against ESD and excess voltage transients.

## Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 54LS08
- Lower power alternative to bipolar logic
- Full Military Temperature Range

## Ordering Information

The following part suffixes apply:

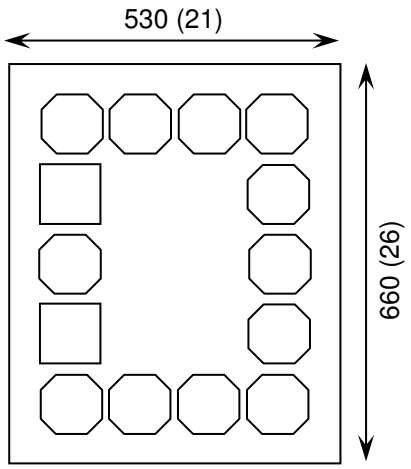
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

## Die Dimensions in µm (mils)




## Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

| | | |
|---|---|---|
| Die Size (Unsawn) | 530 x 660<br>21 x 26 | µm<br>mils |
| Minimum Bond Pad Size | 76 x 76<br>3 x 3 | µm<br>mils |
| Die Thickness | 280 (±20)<br>11.02 (±0.79) | µm<br>mils |
| Top Metal Composition | Al-Si-Cu | |
| Back Metal Composition | N/A – Bare Si | |

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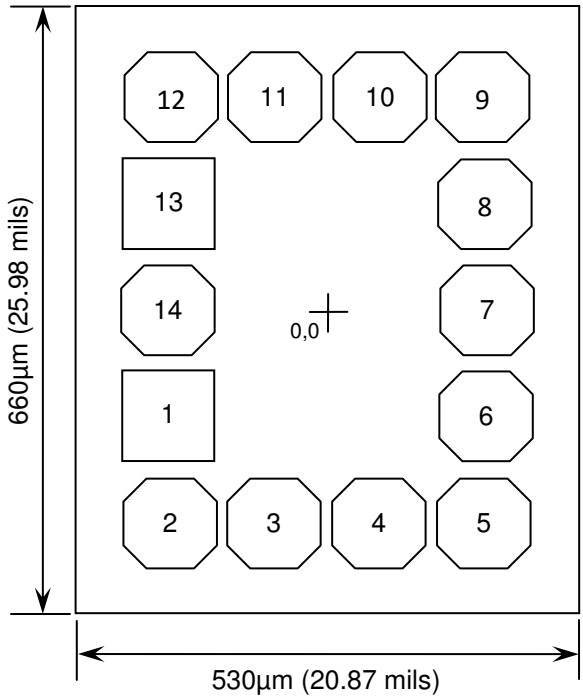
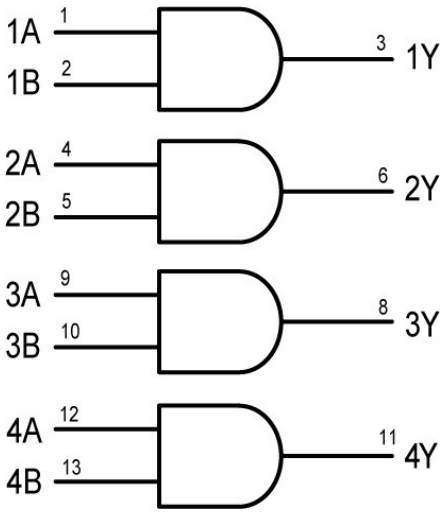
## Pad Layout and Functions




| PAD | FUNCTION | COORDINATES (µm) | |
|---|---|---|---|
| | | X | Y |
| 1 | 1A | -167 | -116 |
| 2 | 1B | -165 | -232 |
| 3 | 1Y | -55 | -232 |
| 4 | 2A | 55 | -232 |
| 5 | 2B | 165 | -232 |
| 6 | 2Y | 167 | -116 |
| 7 | GND | 168 | 0 |
| 8 | 3Y | 167 | 116 |
| 9 | 3A | 165 | 232 |
| 10 | 3B | 55 | 232 |
| 11 | 4Y | -55 | 232 |
| 12 | 4A | -165 | 232 |
| 13 | 4B | -167 | 116 |
| 14 | $V_{CC}$ | -168 | 0 |
| CONNECT CHIP BACK TO $V_{CC}$ OR FLOAT | | | |

## Logic Diagram




## Function Table

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |
| H = High level (steady state)<br>L = Low level (steady state) | | |

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## Absolute Maximum Ratings[1]

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| DC Supply Voltage (Referenced to GND) | $V_{CC}$ | -0.5 to +7.0 | V |
| DC Input Voltage (Referenced to GND) | $V_{IN}$ | -0.5 to $V_{CC}$ +0.5 | V |
| DC Output Voltage (Referenced to GND) | $V_{OUT}$ | -0.5 to $V_{CC}$ +0.5 | V |
| DC Input Current | $I_{IN}$ | ±20 | mA |
| DC Output Current, per pad | $I_{OUT}$ | ±50 | mA |
| DC Supply Current, $V_{CC}$ or GND, per pad | $I_{CC}$ | ±50 | mA |
| Power Dissipation in Still Air[2] | $P_D$ | 750 | mW |
| Storage Temperature Range | $T_{STG}$ | -65 to 150 | °C |

**1.** Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions[3] (Voltages Referenced to GND)

| PARAMETER | | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| DC Supply Voltage | | $V_{CC}$ | 4.5 | 5.5 | V |
| DC Input or Output Voltage | | $V_{IN}$ ,$V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature Range | | $T_J$ | -55 | +125 | °C |
| Output current - High | | $I_{OH}$ | - | -24 | mA |
| Output current - Low | | $I_{OL}$ | - | 24 | mA |
| Input Rise or Fall rate ($V_{IN}$ from 0.8V to 2V) | $V_{CC}$ = 4.5V | Δt/ΔV | 0 | 10 | ns/V |
| | $V_{CC}$ = 5.5V | | 0 | 8 | |

**3.** This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND ≤ ($V_{IN}$ or $V_{OUT}$) ≤ $V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages referenced to GND)

| PARAMETER | SYMBOL | $V_{CC}$ | CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | 25°C | 85°C | FULL RANGE[4] | |
| Minimum High-Level Input Voltage | $V_{IH}$ | 4.5V | $V_{OUT}$ = 0.1V or $V_{CC}$ -0.1V | 2 | 2 | 2 | V |
| | | 5.5V | | 2 | 2 | 2 | |
| Maximum Low-Level Input Voltage | $V_{IL}$ | 4.5V | $V_{OUT}$ = 0.1V or $V_{CC}$ -0.1V | 0.8 | 0.8 | 0.8 | V |
| | | 5.5V | | 0.8 | 0.8 | 0.8 | |
| Minimum Low-Level Output Voltage | $V_{OL}$ | 4.5V | $I_{OUT}$ = 50µA | 0.1 | 0.1 | 0.1 | V |
| | | 5.5V | | 0.1 | 0.1 | 0.1 | |
| | | 4.5V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$[5] $I_{OL}$ = 24mA | 0.36 | 0.44 | 0.50 | V |
| | | 5.5V | | 0.36 | 0.44 | 0.50 | |
| | | 4.5V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$[5,6] $I_{OL}$ = 50mA | - | - | 1.65 | V |
| | | 5.5V | | - | - | 1.65 | |

**4.** -55˚C ≤ $T_J$ ≤ +125˚C **5.** All outputs loaded; thresholds on input associated with output under test. **6.** Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C

## DC Electrical Characteristics Continued (Voltages referenced to GND)

| PARAMETER | SYMBOL | $V_{CC}$ | CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | 25°C | 85°C | FULL RANGE[4] | |
| Minimum High-Level Output Voltage | $V_{OH}$ | 4.5V | $I_{OUT}$ = 50µA | 4.4 | 4.4 | 4.4 | V |
| | | 5.5V | | 5.4 | 5.4 | 5.4 | |
| | | 4.5V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$[5] $I_{OH}$ = -24mA | 3.86 | 3.76 | 3.7 | V |
| | | 5.5V | | 4.86 | 4.76 | 4.7 | |
| Maximum Input Leakage Current | $I_{IN}$ | 5.5V | $V_{IN}$ = $V_{CC}$ or GND | ±0.1 | ±1.0 | ±1.0 | µA |
| Additional Maximum $I_{CC}$ / Input | $\Delta I_{CCT}$ | 5.5V | $V_{IN}$ = $V_{CC}$ -2.1V | 0.6 | 1.5 | 1.6 | mA |
| Minimum Dynamic Output Current[7] | $I_{OLD}$ | 5.5V | $V_{OLD}$ = 1.65V Max | - | 75 | 50 | mA |
| | $I_{OHD}$ | 5.5V | $V_{OHD}$ = 3.85V Min | - | -75 | -50 | |
| Maximum Quiescent Supply Leakage Current | $I_{CC}$ | 5.5V | $V_{IN}$ = $V_{CC}$ or GND $I_{OUT}$ = 0µA | 4 | 40 | 80 | µA |

**7.** Maximum test duration 2ms, one output loaded at a time.

## AC Electrical Characteristics[8] $V_{CC}$ = 5.0V ±0.5V

| PARAMETER | SYMBOL | $V_{CC}$ | CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | 25°C | 85°C | FULL RANGE[4] | |
| Maximum Propagation Delay Input A or B to Output Y (Figure 1) | $t_{PLH}$ | 5.0V | $C_L$ = 50pF, Input tr = tf =3.0ns | 9 | 10 | 11.7 | ns |
| | $t_{PHL}$ | 5.0V | | 9 | 10 | 11.7 | |
| Maximum Input Capacitance | $C_{IN}$ | 5.0V | $T_J$ = 25°C | TYPICAL | | | pF |
| | | | | 4 | | | |
| Power Dissipation Capacitance | $C_{PD}$ | 5.0V | $T_J$ = 25°C, $C_L$ = 50pF | 30 | | | pF |

**8.** Not production tested in die form, characterized by chip design and tested in package.

## Switching Waveform

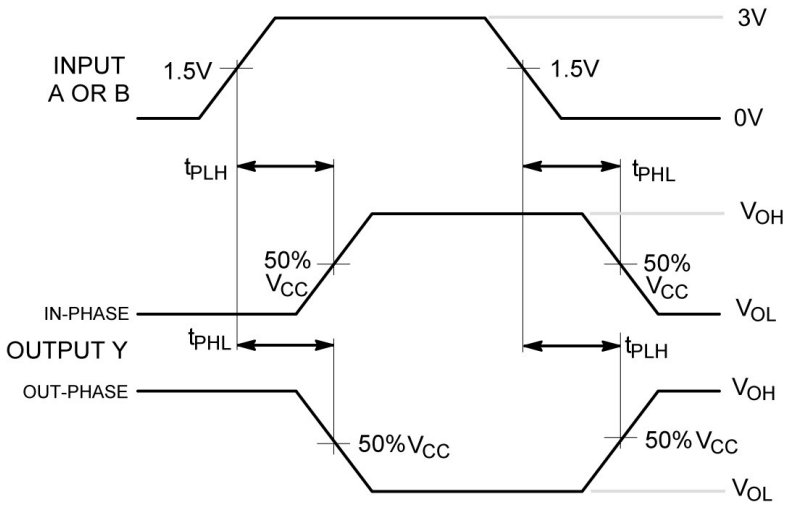
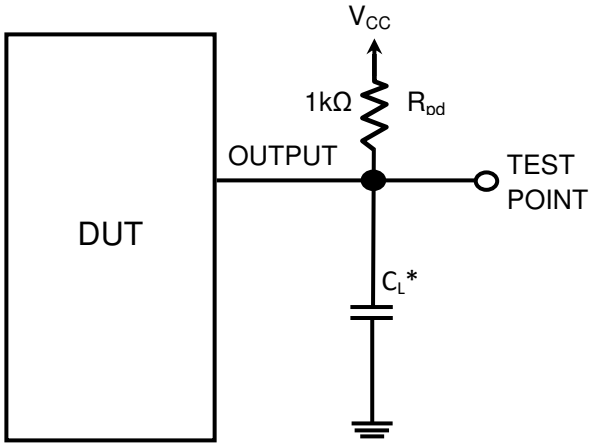



**Figure 1** – Propagation Delay

## Test Circuit




* Includes all probe and jig capacitance

**Figure 2**